REMARKS

In the Office Action, the Examiner notes that claims 1-16 are pending and rejected. By this response, Applicant has cancelled claims 2, 11, and 15, and amended claims 1, 3, 10, and 12. Claims 4-9 and 13-14, and 16 continue unamended. No new matter has been entered.

In view of both the amendments presented above and the following discussion, Applicant submits that none of the claims now pending in the application are anticipated or obvious under the respective provisions of 35 U.S.C. §§102 and 103. Thus, Applicant believes that all of the pending claims are now allowable.

It is to be understood that Applicant, by amending the claims, does not acquiesce to the Examiner's characterizations of the art of record or to Applicant's subject matter recited in the pending claims. Further, Applicant is not acquiescing to the Examiner's statements as to the applicability of the art of record to the pending claims by filing the instant responsive amendments.

REJECTIONS

35 U.S.C. §102

Claims 1, 6, 7, 9, 10 and 14-16

The Examiner has rejected claims 1, 6, 7, 9-10, and 14-16 under 35 U.S.C. § 102(a) as being anticipated by the instant application (specifically Figure 1). The rejection is respectfully traversed.

In particular, the Examiner alleges that, regarding claim 1, the instant application's disclosed prior art shows all of the aspects of Applicant's present invention, including a pair of filters that teach the vector arithmetic structures (VAS) of Applicant's invention. The Applicant respectfully disagrees.

The Applicant respectfully submits that Figure 1 of the instant application fails to teach or suggest each and every element of the claimed invention, arranged as in at least Applicant's amended claim 1. Specifically, the Applicant

submits that Figure 1 of the instant application fails to teach or suggest at least "a plurality of vector registers" and "a vector arithmetic unit" of each vector arithmetic structure. Specifically, Applicant's claim 1 positively recites:

> "An encoder, comprising:
> a constellation generator, responsive to an input bitstream to produce an impulse comprising an in-phase component and a quadrature component, said impulse defining symbols within a constellation of symbols;
> a pair of vector arithmetic structures (VAS), each VAS adapting a respective one of said in-phase and quadrature components to produce respective shaped in-phase and quadrature components, wherein each VAS comprises:
> a plurality of vector registers (VR) for storing precomputed pulse shaping values; and
> a vector arithmetic unit (VAU) for arithmetically processing a selected vector and an accumulated vector, said selected vector comprising a plurality of pre-computed values selected from said vector registers in response to a received component signal; and
> a combiner, for combining said shaped in-phase and quadrature components to produce an encoded bitstream."
> (Emphasis added.)

Applicant's invention of at least claim 1 is directed, at least in part, to an encoder including a pair of vector arithmetic structures (VAS) for adapting a respective one of in-phase and quadrature components to produce respective shaped in-phase and quadrature components. Furthermore, Applicant's invention of at least claim 1, as amended, discloses that each of the VASs comprises a plurality of vector registers and a vector arithmetic unit. Nowhere in Figure 1 of the instant application is there any teaching or suggestion of a pair of vector arithmetic structures. Furthermore, nowhere in Figure 1 of the instant application is there any teaching or suggestion that each of the vector arithmetic structures comprises a plurality of vector registers and a vector arithmetic unit, as taught in Applicant's amended claim 1.

For at least the reasons stated above, Applicant respectfully submits that there is absolutely no teaching or suggestion in Figure 1 of the instant application for an encoder including at least a vector arithmetic structure (VAS) as taught in

Applicant's Specification and claimed by at least Applicant's claim 1. That is, the Applicant respectfully submits that Figure 1 of the instant application absolutely fails to teach or suggest each and every element of at least each of the VASs of Applicant's claim 1 as required for anticipation, and as such does not anticipate at least Applicant's claim 1.

Therefore, Applicant submits that independent claim 1 is not anticipated by the teachings of Figure 1 of the instant application and, as such, fully satisfies the requirements of 35 U.S.C. § 102 and is patentable thereunder. Furthermore, independent claim 10 recites features similar to the relevant features recited in claim 1. As such, Applicant submits that independent claim 10 is also not anticipated by the teachings of Figure 1 of the instant application and also fully satisfies the requirements of 35 U.S.C. § 102 and is patentable thereunder.

Furthermore, dependent claims 6, 7, 9, 14, and 16 depend, either directly or indirectly, from independent claims 1 and 10 and recite additional features therefor. As such, and for at least the reasons set forth herein, Applicant submits that dependent claims 6, 7, 9, 14, and 16 are also not anticipated by the teachings of Figure 1 of the instant application. Therefore, Applicant submits that dependent claims 6, 7, 9, 14, and 16 also fully satisfy the requirements of 35 U.S.C. § 102 and are patentable thereunder.

35 U.S.C. § 103(a)

Claims 2-4, 8, 11 and 12

The Examiner rejected claims 2-4, 8, and 11-12 under 35 U.S.C. § 103(a) as being unpatentable over the instant application in view of Corleto et al. (U.S. Patent 5,668,749, herein "Corleto"). The rejection is respectfully traversed.

Claims 2-4 and 8 depend, either directly or indirectly, from Applicant's claim 1. Claims 11 and 12 depend, directly and indirectly, respectively, from Applicant's claim 10. The Examiner applied Figure 1 of the instant application for his rejection of claims 2-4, 8, and 11-12 as described above for the Examiner's

rejection of Applicant's claims 1 and 10. The Examiner correctly concedes, however, that regarding claims 2, 4, 8, and 11-12, Figure 1 of the instant application does not disclose that the VAS comprises a plurality of vector registers and a vector arithmetic unit. As such, the Examiner cites Corleto for teaching a plurality of registers for storing precomputed values from memories and selected vectors from the in-phase and quadrature registers. The Examiner alleges that it would have been obvious to incorporate the teachings of Corleto into Figure 1 of the instant application. The Applicant respectfully disagrees.

In general, Corleto teaches a circuit for performing arithmetic operations in a demodulator. In Corleto, a circuit for determining a radius value and a phase value from an in-phase signal and a quadrature signal iteratively approximates the phase value and the radius values using the coordinate rotational digital computer (CORDIC) algorithm. The circuit of Corleto includes a multi-task arithmetic unit, memory, and a controller. The multi-task arithmetic unit includes registers, multiplexers, shift registers, and an adder to perform various arithmetic operations. The circuit further includes dynamic memory for storing the solutions of the radius value and phase value at different points in time. (Corleto, Abstract).

Although Corleto discloses various registers and memory, the components of Corleto are arranged in a completely different configuration than Applicant's invention, and produce a completely different result than Applicant's invention. The Applicant's invention is directed, at least in part, towards shaping of in-phase and quadrature components prior to combination of the in-phase and quadrature components for transmission. In particular, Applicant's invention of at least claim 1 includes a VAS for adapting an in-phase component of a received component signal, and a VAS for adapting a quadrature component of the received component signal, to produce respective shaped in-phase and quadrature components. Furthermore, each of the VASs in the Applicant's invention of at least claim 1 includes a vector arithmetic unit for processing a selected vector and an accumulated vector.

In Corleto, on the other hand, processing of the in-phase and quadrature signals is performed at a demodulator to recover the in-phase and quadrature components of the transmitted signal using an iterative approximation technique. As taught in Corleto, however, the processing required in the Corleto system for iteratively approximating radius and phase values to produce successively more accurate radius and phase values is completely different from the processing performed by Applicant's invention of at least claim 1 for shaping in-phase and quadrature components prior to transmission of a combination of the shaped in-phase and quadrature components.

Furthermore, in Corleto, unlike in Applicant's invention of at least claim 1, the in-phase and quadrature signals are processed together in a multi-task arithmetic unit. In particular, in-phase and quadrature components are both passed through a first multiplexer to a first shift register and are both passed through a second multiplexer to a second shift register. An adder performs operations on combinations of in-phase signals and quadrature signals from the first and second shift registers to produce approximate radius and phase values. In the Applicant's invention of at least claim 1, on the other hand, processing of the in-phase and quadrature components is performed independently using a VAS for in-phase component shaping and another VAS for quadrature component shaping prior to combination of the shaped in-phase and quadrature components.

In other words, Corleto teaches processing of shifted combinations of in-phase and quadrature signals for approximating radius and phase values. Thus, use of multiplexers and registers for demodulating combinations of received in-phase and quadrature signals to iteratively approximate radius and phase values, as taught in Corleto, is simply not an in-phase VAS for producing a shaped in-phase component and a quadrature VAS for producing a shaped quadrature component, as taught in Applicant's invention of at least claim 1. Thus, the configuration, processing, and results as taught with respect to the Corleto

system are completely different from the configuration, processing, and results as taught in Applicant's invention of at least claim 1.

Furthermore, Corleto is completely devoid of any teaching or suggestion of vector registers for storing precomputed pulse shaping values, as taught in Applicant's invention of at least claim 1. Rather, the registers of Corleto merely store received in-phase and quadrature signals and multiplexed combinations of the in-phase and quadrature signals, and perform shifting operations on the multiplexed combinations of the in-phase and quadrature signals. Moreover, the accumulator register, as taught in Corleto, does not store precomputed pulse shaping values. Rather, as taught in Corleto, the accumulator register stores iteratively computed radius and phase approximations. Thus, since Corleto fails to teach or suggest the vector registers, Corleto must also fail to teach or suggest a selected vector comprising a plurality of precomputed values selected from the vector registers. As such, Figure 1 of the instant application and Corleto, alone or in combination, fail to teach Applicant's invention of at least claim 1, as a whole.

Moreover, unlike Applicant's invention of at least claim 1, which is directed towards an encoder, Corleto is directed towards demodulation of a signal for determining associated radius and phase values. As such, since Corleto is directed towards demodulation processing, while Applicant's invention is directed towards encoder processing, and for at least the other reasons discussed hereinabove, Applicant submits that there is no suggestion or motivation to combine the teachings of Figure 1 of the instant application and the teachings of Corleto. Additionally, Applicant submits that, even if there were such a motivation or suggestion, the teachings of Corleto cannot be operatively combined with the teachings of the instant Application relied upon by the Examiner for rejecting Applicant's claims.

For prior art reference to be combined to render obvious a subsequent invention under 35 U.S.C. § 103, there must be something in the prior art as a whole which suggests the desirability, and thus the obviousness, of making the combination. Uniroyal v. Rudkin-Wiley, 5 U.S.P.SQ.2d 1434, 1438 (Fed. Cir.

1988). The teachings of the references can be combined only if there is some suggestion or incentive in the prior art to do so. In re Fine, 5 U.S.P.SQ.2d 1596, 1599 (Fed. Cir. 1988). Hindsight is strictly forbidden. It is impermissible to use the claims as a framework to pick and choose among individual references to recreate the claimed invention Id. at 1600; W.L. Gore Associates, Inc., v. Garlock, Inc., 220 U.S.P.Q. 303, 312 (Fed. Cir. 1983). Moreover, the mere fact that a prior art structure could be modified to produce the claimed invention would not have made the modification obvious unless the prior art suggested the desirability of the modification. In re Fritch, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992); In re Gordon, 221 U.S.P.Q. 1125, 1127 (Fed. Cir. 1984).

Applicant submits that there is absolutely no motivation or suggestion in the encoder of Figure 1 of the instant application for the combination of the references. That is, there is nothing in the description of Figure 1 of the instant application that indicates a desire or need for a demodulation radius/phase approximation circuit such as the circuit of Corleto. In addition, Applicant submits that there is also no motivation or suggestion in Corleto for the combination of the references. More specifically, the teachings of Corleto for a circuit for performing arithmetic operations in a demodulator do not suggest or motivate combination of the demodulation circuit of Corleto with the encoder of Figure 1 of the instant application. That is, there is absolutely no teaching, suggestion, or motivation in Corleto for combining the arithmetic circuit of Corleto with an encoder such as the encoder of Figure 1 of the instant application in an attempt to teach the invention of Applicant. Neither Corleto, nor Figure 1 of the instant application, teach or suggest how the arithmetic circuit of Corleto would be capable of operating in the encoder of Figure 1 of the instant application.

Moreover, Applicant submits that even if there was a motivation or suggestion to combine the references (which Applicant believes that there is none), the teachings of Figure 1 of the instant application and Corleto, either alone or in any allowable combination, fail to teach Applicant's invention of at least claim 1. That is, Applicant submits that the teachings of Corleto fail to

bridge the substantial gap between Applicant's invention at least with respect to claim 1, and the teachings of Figure 1 of the instant application.

Therefore, Applicant submits that independent claim 1 is not obvious over the teachings of Figure 1 of the instant application in view of Corleto and, as such, fully satisfies the requirements of 35 U.S.C. § 103 and is patentable thereunder. Furthermore, independent claim 10 recites features similar to the relevant features recited in claim 1. As such, Applicant submits that independent claim 10 is also not obvious over the teachings of Figure 1 of the instant application in view of Corleto and also fully satisfies the requirements of 35 U.S.C. § 103 and is patentable thereunder.

As such, and at least because the teachings of Figure 1 of the instant application and Corleto, alone or in any allowable combination, fail to teach, suggest or make obvious Applicant's claims 1 and 10 for at least the reasons described above, Applicant further submits that the teachings of Figure 1 of the instant application and Corleto, alone or in any allowable combination, also fail to teach, suggest or make obvious Applicant's invention with respect to dependent claims 3-4, 8, 11 and 12, which depend either directly or indirectly from Applicant's claims 1 and 10, respectively and recite further limitations thereof. Therefore, Applicant respectfully submits that claims 3-4, 8, 11 and 12, as they now stand, fully satisfy the requirements of 35 U.S.C. § 103 and are patentable thereunder.

CONCLUSION

Thus, Applicant submits that none of the claims presently in the application are anticipated under the provisions of 35 U.S.C. § 102 or obvious under the provisions of 35 U.S.C. § 103. Consequently, Applicant believes that all of these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If however, the Examiner believes that there are any unresolved issues requiring adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Eamon J. Wall, Esq. at (732) 530-9404 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

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